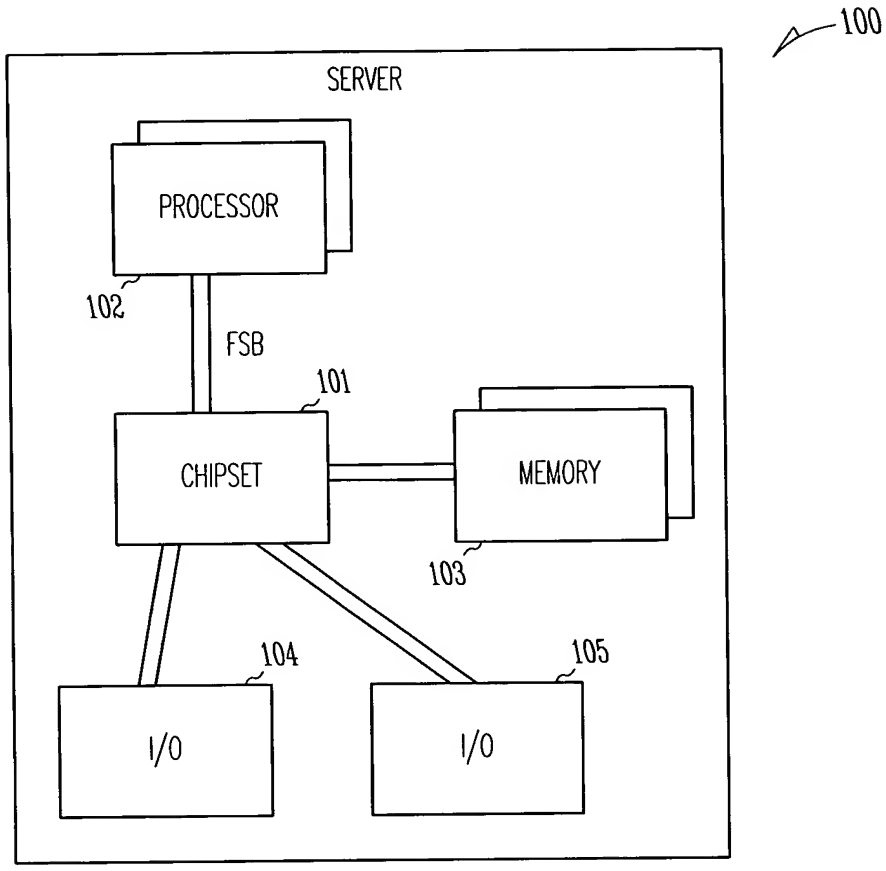
100
SERVER
PROCESSOR
102
FSB
101
CHIPSET
MEMORY
103
104
105
I/O
I/O

Fig. 1

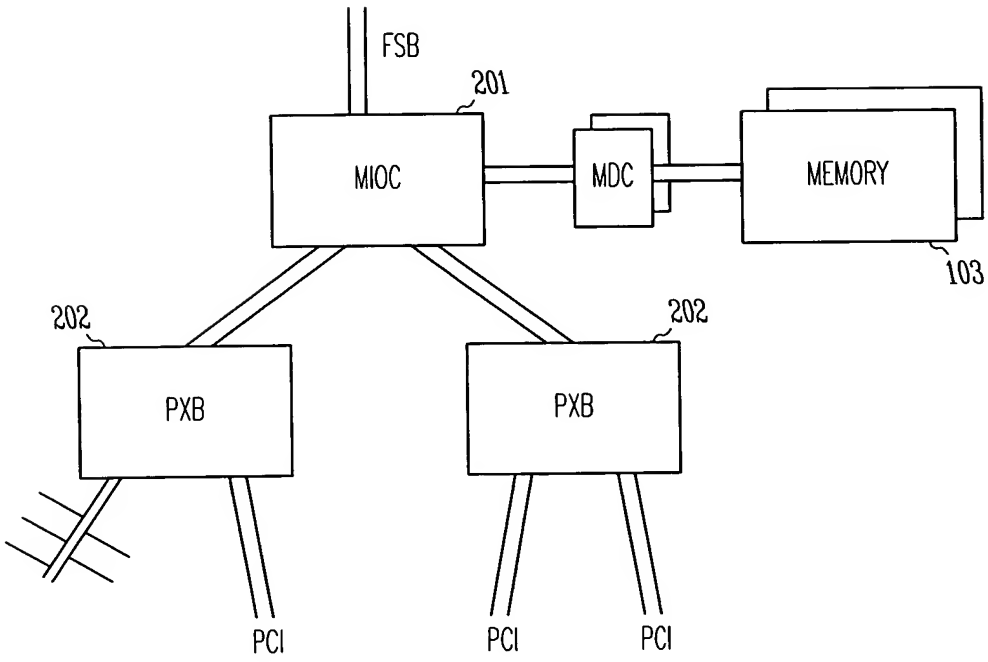

Fig. 2

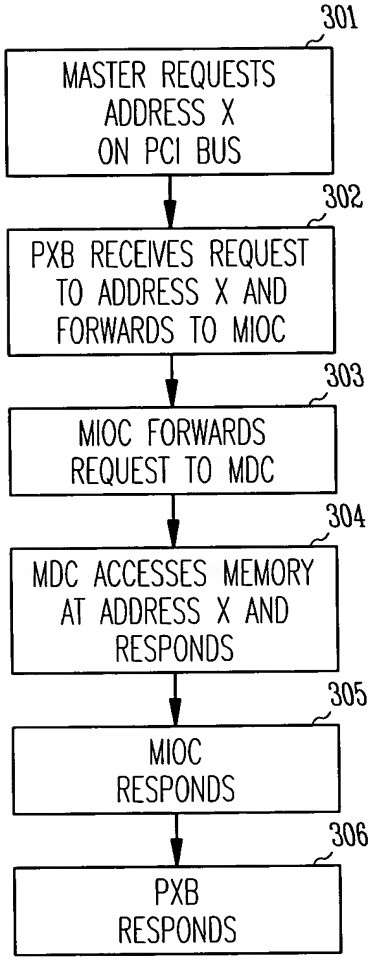
301
MASTER REQUESTS ADDRESS X ON PCI BUS
302
PXB RECEIVES REQUEST TO ADDRESS X AND FORWARDS TO MIOC
303
MIOC FORWARDS REQUEST TO MDC
304
MDC ACCESSES MEMORY AT ADDRESS X AND RESPONDS
305
MIOC RESPONDS
306
PXB RESPONDS

Fig. 3

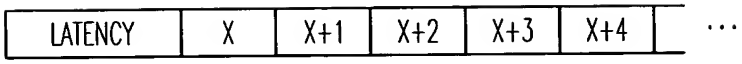
LATENCY
X
X+1
X+2
X+3
X+4
...

Fig. 4

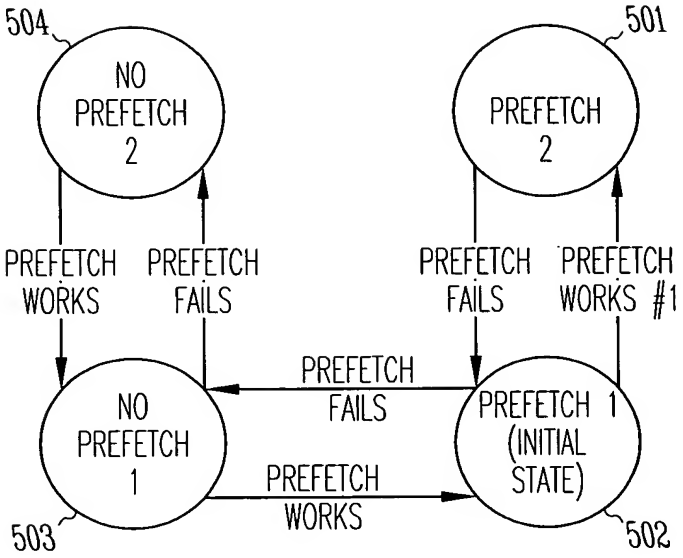
504
NO PREFETCH 2
501
PREFETCH 2
PREFETCH WORKS
PREFETCH FAILS
PREFETCH FAILS
PREFETCH WORKS #1
PREFETCH FAILS
NO PREFETCH 1
PREFETCH 1 (INITIAL STATE)
PREFETCH WORKS
503
502

Fig. 5

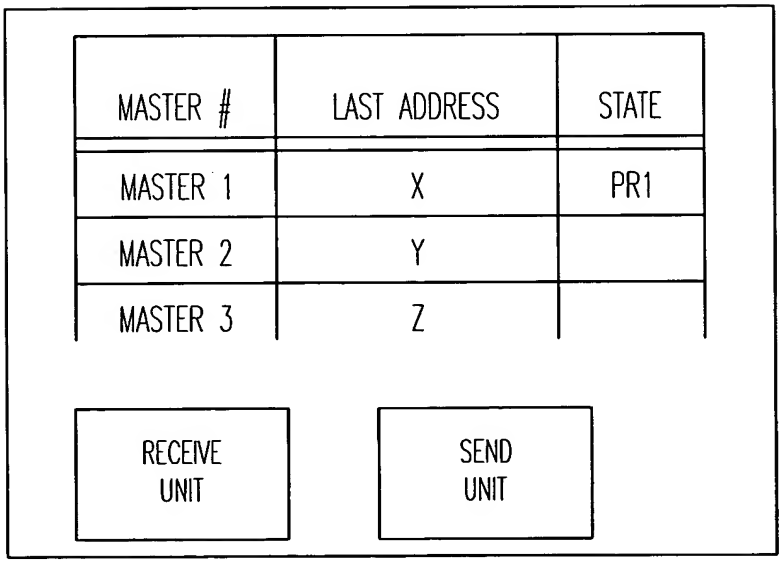
MASTER #
LAST ADDRESS
STATE
MASTER 1
X
PR1
MASTER 2
Y
MASTER 3
Z
RECEIVE UNIT
SEND UNIT

Fig. 6

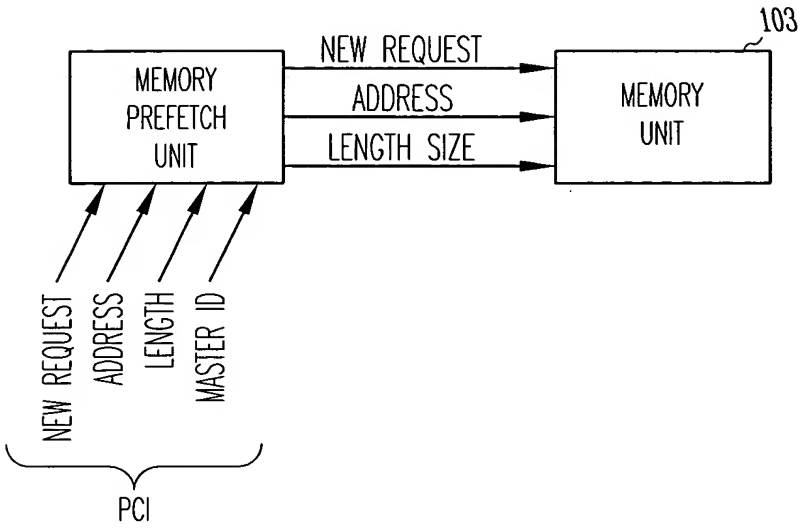
103
MEMORY PREFETCH UNIT
NEW REQUEST
ADDRESS
LENGTH SIZE
MEMORY UNIT
NEW REQUEST
ADDRESS
LENGTH
MASTER ID
PCI

Fig. 7